



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,540	11/20/2001	Thomas Lang	004501-616	8959

7590

02/04/2003

Robert S. Swecker
BURNS, DOANE, SWECKER & MATHIS, L.L.P.
P.O. Box 1404
Alexandria, VA 22313-1404

EXAMINER

CHAMBLISS, ALONZO

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 02/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/988,740

Applicant(s)

PIHLAJA, PEKKA JUHANA

Examiner

Alonzo Chambliss

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 November 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 November 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. Pre-amendment A filed on 11/20/01 has been fully considered and made of record in Paper No. 5. Also, the substitute specification has been fully considered and made of record in Paper No. 4.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 11/20/10 was filed before the mailing date of the non-final rejection on 11/20/01. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

4. The drawings are objected to because reference numeral 16 in Fig. 3 is pointed to the wrong contact spring rather than the center contact spring. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

5. The abstract of the disclosure is objected to because the essential elements "first and second contact springs" are not present in the abstract. Correction is required. See MPEP § 608.01(b).

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: "HIGH-POWER SEMICONDUCTOR MODULE UTILIZING SPRING CONTACTS FOR INCREASE ELECTRICAL ISOLATION".

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

8. Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. In claim 1, the phrase "establishing electrical contacts" is vague and indefinite since it is not clear where the electrical contacts are located relative to the base plate or the chips.

10. In claim 1, the phrase "and have a cover plate" is vague and indefinite since it is not clear where the cover plate is located. Furthermore, is the cover plate on the chip or the base plate.

11. In claim 1, the phrase "their upper face" is vague and indefinite since it is clear if applicant is referring to the chip or the base plate.

12. In claim 1, the phrase "establishing second electrical contacts" is vague and indefinite since it is not clear where the second electrical contacts are located relative to the base plate or the chips.

13. In claim 1, the phrase "electrically isolated" is vague and indefinite since it is not clear how the base plate and the cover plate are electrically isolated. Furthermore, there is no structure in the claim for electrically isolation.

14. In claim 6, the phrase "a third electrical contact" is vague and indefinite since it is not clear what structure in the claim creates the electrical contact.

15. In claim 7, the phrase "a second contact spring" is vague and indefinite since it is not clear where the first contact spring is located.

16. In claim 8, the phrase "on whose inner face a first metallic contact plate is arranged, via which the second electrical contacts with the semiconductor chips are established" is vague and indefinite since it is not clear where the second electrical contacts is relative to the first metallic contact plate.

17. In claim 8, the phrase "from it" is vague and indefinite since it is not clear what it is.

18. In claim 8, the phrase "electrically isolated" is vague and indefinite since it is not clear what is electrically isolated from what. Furthermore, there is no structure in the claim for electrically isolation.

19. In claim 13, the word " use " is vague and indefinite since it not clear from the claim what use is referring to.

20. In claim 13, the phrase " applied to it in the stack " is vague and indefinite since it is not clear what " it " is.

Claim Rejections - 35 USC § 102

21. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

22. Claims 1, 2, and 13, insofar as definite, are rejected under 35 U.S.C. 102(b) as being clearly anticipated by IBM Technical Disclosure Bulletin.

With respect to Claim 1, the IBM disclosure teaches a high-power semiconductor module, in which a number of flat semiconductor chips 10 rest with their lower faces flat on a base plate 12 (i.e. substrate). First electrical contacts are established between the chips 10 and the base plate 12. A cover plate 16, which is arranged parallel to the base plate 12 is applied to the upper face of the chips 10. Second electrical contacts are established between the chips 10 and the cover plate 16. The outer faces of the base plate and of the cover plate (i.e. the area of the base and cover plate that are fasten to one another by screws) which face away from the semiconductor chips 10 are each electrically isolated from the semiconductor chips 10 (see English translation and Figs. 1, 1A, and 1B).

With respect to Claim 2, the IBM disclosure teaches wherein a first electrically conductive, elastic connecting element, preferably in the form of first contact spring 20 is arranged between the upper face of each semiconductor chip 10 and the cover plate 16 (see Fig. 1).

With respect to Claim 13, the IBM disclosure teaches in which the high-power semiconductor module is arranged together with a cooling apparatus 31, which is adjacent to the outer face of the base plate 12 to form a stack, while maintaining pressure to the stack (i.e. the base plate, chips, and cover plate) (see English translation and Figs. 1, 1a, and 1b).

Claim Rejections - 35 USC § 102

23. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

24. Claims 1-6 and 10-13, insofar as definite, are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hiyoshi (U.S. 6,297,549).

With respect to Claim 1, Hiyoshi teaches a high-power semiconductor module, in which a number of flat semiconductor chips 361, 362 rest with their lower face flat on a

base plate 31, 331, 332 (i.e. substrate). First electrical contacts are established between the chips 361, 362 and the base plate 31, 331, 332. A cover plate 38, which is arranged parallel to the base plate 31, 331, 332 is applied to the upper face of the chips 361, 362. Second electrical contacts are established between the chips 361, 362 and the cover plate 38. The outer faces of the base plate 31, 331, 332 and of the cover plate 38, which face away from the semiconductor chips 361, 362 are each electrically isolated from the semiconductor chips 361, 362 (see col. 6 lines 43-67 and col. 7 lines 15-45; Fig. 2B).

With respect to Claim 2, Hiyoshi teaches wherein a first electrically conductive, elastic connecting element, preferably in the form of first contact spring 37 is arranged between the upper face of each semiconductor chip 361, 362 and the cover plate 38 (see Fig. 2B).

With respect to Claim 3, Hiyoshi teaches a base plate 31, 331, 332 comprises an electrically insulating substrate 31, which has a first metal 331 coating on the inner face, wherein the semiconductor chips 362 are mounted, preferably by techniques such as soldering 341, 342 on the first metal coating 331 (see Fig. 2B).

With respect to Claim 4, Hiyoshi teaches wherein the substrate is composed of a ceramic, preferably an AlN ceramic (see col. 4 lines 5-9).

With respect to Claim 5, Hiyoshi teaches wherein the base plate 31, 331, 332 is provided with a second metal coating 332 on the outer face (see Fig. 2).

With respect to Claim 6, Hiyoshi teaches wherein in an area located outside the semiconductor chips 361, 362 pressure is applied by a conductive pillar 40, 41 to the

first metal coating 361 by the cover plate 38 thus establishing a third electrical contact (see col. 8 lines 19-50; Figs. 2C and 2F).

With respect to Claim 10, Hiyoshi teaches wherein an electrically insulating housing 59 is arranged between the base plate 31 and the cover plate 54 while enclosing the semiconductor chips 81, 82 and the associated contact devices (see col. 12 lines 1-13; Fig. 4).

With respect to Claim 11, Hiyoshi teaches wherein the semiconductor chips 361, 362 are connected electrically in parallel within the high-power semiconductor module (see col. 5 lines 14-35).

With respect to Claim 12, Hiyoshi teaches wherein at least some of the semiconductor chips 361, 362 are controllable semiconductor switches, in particular IGBTs (see col. 4 lines 10-15 and 40-47).

With respect to Claim 13, Hiyoshi teaches in which the high-power semiconductor module is arranged together with a cooling apparatus 60, which is adjacent to the outer face of the base plate 31 to form a stack, while maintaining pressure to the stack (i.e. the base plate, chips, and cover plate) (see col. 11 lines 30-54; Fig. 4).

Allowable Subject Matter

25. Claim 7 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not teach or suggest the combination wherein the third electrical contact is established via a second electrically conductive elastic connecting element preferably in the form of a second contact spring.

The prior art made of record and not relied upon is cited primarily to show the product of the instant invention.

Conclusion

26. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (703) 306-9143. The fax phone number for this Group is (703) 308-7722 or 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956.

AC/January 7, 2003


Alonzo Chambliss
Patent Examiner
Art Unit 2827